Additional Topics for the Final Exam

CS 315-01

Spring, 2016

In addition to the possible topics from the two midterms, the following topics may be covered on the final exam.

• Implementation of jump instruction in “giant cycle” processor.

• Basic design of pipelined MIPS processors: interpolate registers between the stages.

• Pipeline diagrams.

• Pipeline hazards
  – Structural
  – Data Hazards
    * Forwarding EX to EX, EX to MEM, MEM to EX
    * Writeback to register for earlier instruction can overlap register-read for later instruction
    * Stalls, NOPs
    * Compiler reordering
  – Control Hazards
    * Branch decision in EX stage vs ID stage
    * Branch taken vs fall-through.
    * Static branch prediction
    * Dynamic branch prediction
    * Delayed branches, delay slots

• Cache
  – Memory hierarchy
  – Principle of temporal and spatial locality
  – Cache line/block
  – Collision, eviction
  – Hit, miss, hit rate, miss rate, hit time, miss penalty.
- Direct-mapped cache.
- Valid bit, tag, set, index, word offset (block offset in text), byte offset, way.
- Actual cache size vs data storage size
- Miss rate vs cache size, line size
- Miss rate and memory access time
- Early restart, critical/requested word first
- Handling a read hit/miss
- Write-through vs write-back cache
- Write buffers
- Write-allocate vs no-write-allocate
- Dirty bit
- Split vs unified caches
- Memory stall cycles, AMAT
- N-way set-associative caches, fully associative cache.
  * Effect of set size on miss rate.
  * Replacement scheme: least recently used, random, or some less expensive variant of LRU